We claim:

1. A switching system, comprising:

a clock signal having a rising edge and a falling edge;

2^K data inputs and 2^K data select signals;

K layers of switches, wherein each j^{th} layer is configured to receive $2^{K-(j-1)}$ data inputs and propagate 2^{K-j} of the $2^{K-(j-1)}$ data inputs, wherein each j^{th} layer is further configured to receive $2^{K-(j-1)}$ data select signals and propagate 2^{K-j} of the $2^{K-(j-1)}$ data select signals, wherein each layer comprises 2^{K-j} switches, wherein each of the 2^{K-j} switches comprises:

a logical OR gate configured to receive at least two select signals and generate a data valid signal;

a multiplexer (MUX) configured to receive at least two data input signals and one of the at least two select signals, the MUX further configured to generate a data output;

a first flip flop configured to receive the data valid signal and release the data valid signal in response to the rising edge of the clock signal; and

a second flip flop configured to receive the data output and release the data output in response to the rising edge of the clock signal.

2. A switching system, comprising:

a clock signal having a rising edge and a falling edge;

switches, wherein each switch comprises:

a logical OR gate configured to receive at least two select signals and generate a data valid signal;

a multiplexer (MUX) configured to receive at least two data input signals and one of the at least two select signals, the MUX further configured to generate a data output; and

a first flip flop configured to receive the data valid signal and release the data valid signal in response to the rising edge of the clock signal;

a second flip flop configured to receive the data output and release the data output in response to the rising edge of the clock signal;

up to 2^K data inputs and up to 2^K data select signals;

a first layer of switches having 2^{K-1} switches, wherein the first layer is configured to receive the up to 2^K data inputs and propagate 2^{K-1} of the up to 2^K data inputs, wherein the first layer is further configured to receive the up to 2^K data select signals and propagate 2^{K-1} of the up to 2^K data select signals; and

K-1 additional layers of switches, wherein each j^{th} layer of the K-1 additional layers is configured to receive $2^{K-(j-1)}$ data inputs and propagate 2^{K-j} of the $2^{K-(j-1)}$ data inputs, wherein each j^{th} layer is further configured to receive $2^{K-(j-1)}$ data select signals and propagate 2^{K-j} of the $2^{K-(j-1)}$ data select signals, wherein each K-1 additional layer comprises 2^{K-j} switches.

3. A switch comprising:

a clock having a clock signal;

a logical OR gate having two OR inputs and an OR output;

a first flip-flop configured to receive the OR output and propagate the OR output in response to the clock signal;

a multiplexer (MUX) having a first MUX input, a second MUX input, a MUX output, and a MUX select, wherein the MUX select is one of the two OR inputs; and

a second flip-flop configured to receive the MUX output and propagate the MUX output in response to the clock signal.

4. A switch comprising:

a logical OR gate configured to receive at least two select signals and generate a data valid signal;

a multiplexer (MUX) configured to receive at least two data input signals and one of the at least two select signals, the MUX further configured to generate a data output;

a first flip flop configured to receive the data valid signal and release the data valid signal in response to a clock signal; and

a second flip flop configured to receive the data output and release the data output in response to the clock signal.

5. The system of claim 4, wherein the first flip flop is configured to release the data valid signal in response to a rising edge of the clock signal.

6. The system of claim 4, wherein the first flip flop is configured to release the data valid signal in response to a falling edge of the clock signal.

7. The system of claim 4, wherein the second flip flop is configured to release the data output in response to a rising edge of the clock signal.

8. The system of claim 4, wherein the second flip flop is configured to release the data output in response to a falling edge of the clock signal.

9. A system, comprising:

data select signals;

data inputs; and

a switching system configured to receive the data select signals and the data inputs, the switching system further configured to produce a data valid signal in response to the received data select signals, the switching system further configured to generate a data output from the data inputs in response to the data select signals.

10. The system of claim 9, wherein the switching system comprises a plurality of switches.

11. The system of claim 10, wherein each of the plurality of switches comprises:

a logical OR gate configured to receive at least two select signals and generate a data valid signal;

a multiplexer (MUX) configured to receive at least two data input signals and one of the at least two select signals, the MUX further configured to generate a data output;

a first flip flop configured to receive the data valid signal and release the data valid signal in response to a clock signal; and

a second flip flop configured to receive the data output and release the data output in response to the clock signal.

12. The system of claim 11, wherein the first flip flop is configured to release the data valid signal in response to a rising edge of the clock signal.

13. The system of claim 11, wherein the first flip flop is configured to release the data valid signal in response to a falling edge of the clock signal.

14. The system of claim 11, wherein the second flip flop is configured to release the data output in response to a rising edge of the clock signal.

15. The system of claim 11, wherein the second flip flop is configured to release the data output in response to a falling edge of the clock signal.

16. A switching method comprising the steps of:

(a) receiving a number of data inputs and a number of data select signals, wherein the number of data inputs and the number of data select signals is the same;

(b) choosing at least half of the received data inputs and at least half of the received data select signals, wherein the chosen number of data inputs and the chosen number of data select signals is the same, wherein the at least half of the received data inputs and at least half of the received data select signals is a power of 2;

(c) outputting the chosen data inputs and the chosen data select signals;

(d) sequentially repeating steps (a) through (c) until only one data input and only one data select signal is outputted.

17. A method comprising the steps of:

(a) receiving a number of data inputs;

(b) choosing at least half of the received data inputs; and

(c) outputting the chosen data inputs.

18. The method of claim 17, wherein the step of choosing at least half of the received data inputs comprises the step of selecting a number of received data inputs such that the selected number of received data inputs is a power of 2.

19. The method of claim 17, further comprising the step of repeating steps (a) through (c) until only one data input is outputted.

20. The method of claim 17, further comprising the steps of:

(d) receiving a number of data select signals;

(e) choosing at least half of the received data select signals; and

(f) outputting the chosen data select signals.

21. The method of claim 20, wherein the step of choosing at least half of the received data select signals comprises the step of selecting a number of received data selects signals such that the selected number of received data select signals is a power of 2.

22. The method of claim 20, further comprising the step of repeating steps (d) through (f) until only one data select signal is outputted.

23. The method of claim 20, wherein step (d) and step (f) are responsive to a clock signal having a rising edge and a falling edge.

24. The method of claim 23, wherein step (d) and step (f) are further responsive to the rising edge of the clock signal.

25. The method of claim 23, wherein step (d) and step (f) are further responsive to the falling edge of the clock signal.

26. A switching system comprising:

means for receiving a number of data inputs and a number of data select signals, wherein the number of data inputs and the number of data select signals is the same;

means for choosing at least half of the received data inputs and at least half of the received data select signals, wherein the chosen number of data inputs and the chosen number of data select signals is the same, wherein the at least half of the received data inputs and at least half of the received data select signals is a power of 2; and

means for outputting the chosen data inputs and the chosen data select signals;

27. A switch comprising:

means for receiving a number of data inputs;

means for choosing at least half of the received data inputs; and

means for outputting the chosen data inputs.

28. The switch of claim 27, wherein the means for choosing at least half of the received data inputs comprises means for selecting a number of received data inputs such that the selected number of received data inputs is a power of 2.

29. The switch of claim 27, further comprising:

means for receiving a number of data select signals;

means for choosing at least half of the received data select signals; and

means for outputting the chosen data select signals.

30. The switch of claim 29, wherein the means for choosing at least half of the received data select signals comprises means for selecting a number of received data selects signals such that the selected number of received data select signals is a power of 2.

31. A switch comprising:

means for receiving at least two select signals;

means for generate a data valid signal from the at least two select signals;

means for receiving at least two data input signals and one of the at least two select signals;

means for generating a data output from the at least two data input signals in response to the one of the at least two select signals;

means for receiving the data valid signal;

means for releasing the data valid signal in response to a clock signal;

means for receiving the data output; and

means for releasing the data output in response to the clock signal.

32. A system, comprising:

data select signals;

data inputs; and

means for receiving the data select signals and the data inputs;

means for producing a data valid signal in response to the received data select signals; and

means for generating a data output from the data inputs in response to the data select signals.